SRI VENKATESWARA COLLEGE OF ENGINEERING

(AUTONOMOUS)

Karakambadi Road, Tirupati-517507

R24

EXAMINATION BRANCH

M.Tech III Semester (R24) Regular Examinations November-2025

TIME TABLE

Exam Timings: **10.00 AM TO 1.00 PM**

Date/Day	VLSI Design (VLSI D)	Computer Science and Engineering (CSE)
24-11-2025 (Monday)	Bi-CMOS Technology and Applications EC24DPE301	Software Defined Networks CS24DPE301
	Optimization Techniques and Applications in VLSI Design EC24DPE302	Reinforcement Learning CS24DPE302
	System on Chip Architecture EC24DPE303	Data Analytics CS24DPE303
26-11-2025 (Wednesday)	Embedded System Design EC24DOE301	Industrial Safety ME24DOE301
	Foundations of Artificial Intelligence EC24DOE302	Business Analytics BA24DOE301
	Introduction to Industry 4.0 and Industrial Internet of Things EC24DOE303	Optimization Techniques MA24DOE301
	Natural Language Processing EC24DOE304	***

Note: Any discrepancy in this time table may be brought to the notice of the under signed immediately.

CONTROLLER OF EXAMINATIONS

Date: 10-11-2025

PRINCIPAL